

Patent Citation Commands on Questel•Orbit

Questel Orbit offers three citation commands :

- **CITF** does a forward citation search for a set of records.
- **CITB** does a backward citation search for a set of records.
- **FAMCITE** creates a citation report for a patent family.

■ The CITF and CITB Commands : Using patent citations to expand a search result with precision

The CITF and CITB commands will find more patent results that are relevant to your search by using the citations that are included on patent publications.

The **CITF** command retrieves subsequent patents that are citing the patents in your initial set. The new result set contains both the original patents and the citing patents.

The **CITB** command retrieves the previously published patents cited by the patents in your initial set. The new set contains both the original patents and the cited patents.

The correct search syntax is to enter the command followed by your search set number, e.g., **CITF SS 1**. The maximum initial set size for both commands is 1,000 records.

These two commands are available in the following databases :

- EPPATENT, European Patents
- FRPATENT, French Patents
- WOPATENT, PCT Applications
- USPAT, U.S. Patents
- DEPAT, German Patents and Utility Models
- PLUSPAT, Worldwide Patents

When searching in Cluster mode, you may use these commands by entering the FROM parameter followed by the the name of one of the databases in the cluster. Example: **CITF SS 1 FROM EPPATENT**

There is no charge for use of the CITF and CITB commands.

Examples

Selected database: USPAT

Search statement 1

MCGREW/IN AND WRIGLEY/PA

** SS 1: Results 19

Search statement 2

CITF SS 1

** SS 2: Results 123

Search statement 3

PRT

1/123 USPAT - (C) USPTO

PN - US6379652 B1 20020430
TI - Oral compositions for reducing mouth odors
IN - Liu, Xiaoyan; Highland Park NJ [US]
- Williams, Malcolm; Piscataway NJ [US]
- Subramanyam, Ravi; Belle Mead NJ [US]
- Hughes, John; Cranbury NJ [US]
PA - Colgate Palmolive Company, New York NY [US]
PCLO- 424049000
PCLX- 424058000
IC - A61K-007/16 A61K-007/26

Search statement 3

CITB SS 1

** SS 3: Results 258

Search statement 4

PRT

1/258 USPAT - (C) USPTO
PN - US6264999 B1 20010724
TI - Chewing gum containing erythritol and method of making
IN - Yatka, Robert J.; Orland Park IL [US]
- Patel, Mansukh M.; Downers Grove IL [US]
- Tyrpin, Henry T.; Palos Heights IL [US]
- Broderick, Kevin B.; Berwyn IL [US]
PA - Wm. Wrigley Jr. Company, Chicago IL [US]
PCLO- 426003000
IC - A23G-003/30

■ The FAMCITE Command: Automatic display of citations

The FAMCITE command is available in the PlusPat database, which has citations for US, EP, WO and FR patents. After conducting a family search for a single patent family, you can display a complete citation report with the FAMCITE command. The report display in three parts :

- The original source family
- The citing patent families (families with a patent citing a member of the source family)
- The cited patent families (families with a patent cited by a member of the source family)

The results in all three sections show complete families. These fields are included for each family in the citation report :

- PN Number and date of publication of all members
- TI English title of the first member
- OTI Non-English title of the first member
- PA Applicant of the first member
- IN Inventor of the first member
- AP Application numbers of all members
- PR Priority numbers of all members
- CT Citations of members EP, WO, US and FR
- AB Summary of first member

You can also display clipped images by adding the parameter IMG. The complete command syntax is **FAMCITE IMG**.

The FAMCITE command can not be used with the LEGAL or FULLTEXT display options.

The FAMCITE command has a flat rate of \$15 per use of the command. All records displayed are included in the flat rate charge, except for the optional image displays which are charged at the normal rate.

Example

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Search statement 1

FAM US5898235/PN

1 Patent Groups

** SS 1: Results 2

Search statement 2

FAMCITE

<< Citation report >>

<< Source Patent Family >>

1/1 PLUSPAT - (C) QUESTEL-ORBIT- image
CPIM (C) Questel-Orbit
PN - US5898235 A 19990427 [US5898235]
      JP10214487 A 19980811 [JP10214487]
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TI - (A) Integrated circuit with power dissipation control
PA - (A) ST MICROELECTRONICS INC (US)
IN - (A) MCCLURE DAVID C (US)
AP - 1996US-0775611; 1997JP-0354340
PR - 1996US-0775611
CT - (US5898235)
US4683382; US5167024; US5483464; US5513361
AB - (US5898235)
An integrated circuit device such as an SRAM operating in a battery backup mode, or operating in a quiescent mode when deselected in the operation of a portable electronic device, includes a power dissipation control circuit that reduces the voltage on an internal power supply node so that the memory array is powered at a minimum level sufficient to retain the data stored therein intact.

<< Citing Patents: Subsequent Patents Citing Source Family >>

1/3 PLUSPAT - (C) QUESTEL-ORBIT
PN - US6377681 B1 20020423 [US6377681]
TI - (B1) Signal line driving circuit with self-controlled power dissipation
PA - (B1) NAT SEMICONDUCTOR CORP (US)
IN - (B1) BREMNER DUNCAN JAMES (GB)
AP - 1998US-0053110
PR - 1998US-0053110
CT - (US6377681)
US5138658; US5323461; US5428682; US5881129; US5898235; US5912513;
US6005934
AB - (US6377681)
A signal line driving circuit with power control for selectively reducing internal power dissipation when driving an external load. While driving the external load with a constant current the output voltage generated across such load is monitored. If the load impedance decreases sufficiently to cause the output voltage to fall below a predetermined threshold value and, therefore, cause the voltage across the signal line driving circuit to increase, the magnitude of the power supply voltage is automatically reduced, thereby reducing the voltage across the signal line driving circuit. Such a signal line driving circuit is particularly advantageous as a subscriber line interface circuit (SLIC). As the subscriber goes from an on-hook condition to an off-hook condition and if the subscriber loop is sufficiently short (or low in impedance), a lower power supply voltage is used to minimize the power dissipation of the SLIC while still maintaining the required subscriber loop current.

2/3 PLUSPAT - (C) QUESTEL-ORBIT
PN - US2001028270 A1 20011011 [US20010028270]
US6396336 B2 20020528 [US6396336]
US6333671 B1 20011225 [US6333671]
TI - (B1) Sleep mode VDD detune for power reduction
PA - (B1) IBM (US)
IN - (B1) ROBERTS ALAN L (US); WISTORT REID A (US)
AP - 1999US-0433279; 2001US-0883048
PR - 1999US-0433279; 2001US-0883048
CT - (US6333671)
US4130899; US4683382; US4691123; US4716463; US5077518; US5477279;
US5511026; US5530398; US5663919; US5747977; US5773966; US5898235;
US6049245; US6118267; JP6-175956
- "Leakage Current Reduction/Minimization through Substrate and/or Well Bias Control Coupled with Clock Power Management", IBM Technical Disclosure Bulletin, vol. 41 No. 01, Jan. 1998, pp. 547-549.

CT - (US20010028270)
US4130899; US4683382; US4691123; US4716463; US5077518; US5477279;
US5511026; US5530398; US5663919; US5747977; US5773966; US5898235;
US6049245; US6118267; JP6-175956

AB - (US6333671)

The leakage current on a semiconductor is reduced while the semiconductor is in a sleep mode. This is accomplished by (1) placing the semiconductor in the sleep mode; (2) providing the semiconductor an internal supply voltage derived from an external supply voltage applied to the semiconductor chip (where the internal supply voltage is less in quantity than the external supply voltage); and (3) reducing the internal supply voltage when the semiconductor enters the sleep mode from an activated mode and returning the internal supply voltage to an activated mode level when the semiconductor returns to the activated mode. The reducing step includes supplying the external supply voltage to a reference circuit which outputs therefrom a reference voltage; and supplying the reference voltage to a regulator, where the regulator attempts to match the reference voltage and outputs therefrom the internal supply voltage. The reference circuit reduces the reference voltage when the semiconductor enters the sleep mode from an activated mode and returns the reference voltage to the activated mode level when the semiconductor returns to the activated mode. The reducing step can be performed by reducing the current flow to one or more diodes in the reference circuit when the semiconductor enters the sleep mode from the activated mode, and increasing the current flow to the diodes when the semiconductor reenters the activated mode from the sleep mode.

3/3 PLUSPAT - (C) QUESTEL-ORBIT- image

CPIM (C) JPO

PN - US6294404 B1 20010925 [US6294404]
JP2001155487 A 20010608 [JP2001155487]

TI - (B1) Semiconductor integrated circuit having function of reducing a power consumption and semiconductor integrated circuit system comprising this semiconductor integrated circuit

PA - (B1) MITSUBISHI ELECTRIC CORP (US)

IN - (B1) SATO HIROTOSHI (JP)

AP - 2000US-0568058; 1999JP-0339609

PR - 1999JP-0339609

CT - (US6294404)

US5265060; US5543649; US5898235; US5955904; JP10-214487

AB - (US6294404)

A semiconductor integrated circuit according to the present invention comprises a synchronous SRAM, a signal generation circuit generating a chip selection signal, a clock signal etc. supplied to the synchronous SRAM, a voltage set circuit setting the voltage of a system power supply line and a controller controlling the signal generation circuit and the voltage set circuit. When setting the synchronous SRAM in a power down mode, the chip selection signal is set in a nonselective state and the power supply voltage of the system power supply line is stepped down to a standby potential. Thus, the synchronous SRAM enters a standby state having extremely low power consumption.

<< Cited Patents: Previous Patents Cited by Source Family >>

1/4 PLUSPAT - (C) QUESTEL-ORBIT- image

CPIM (C) Questel-Orbit

PN - US5513361 A 19960430 [US5513361]

TI - (A) Method and apparatus for reducing power consumption of a fan in a computer system

PA - (A) INTEL CORP (US)
IN - (A) YOUNG BRUCE A (US)
AP - 1994US-0279544
PR - 1994US-0279544
CT - (US5513361)
US4151611; US4279020; US4293927; US4381552; US4615005; US4642441;
US4698748; US4712196; US4809163; US4842431; US4980836; US5247805
AB - (US5513361)
A circuit for controlling power consumption of a fan within a computer system having a central processing unit (CPU) is described. The circuit includes a filter circuit coupled to receive a periodical pulse signal for detecting duty cycle of the periodical pulse signal by converting the periodical pulse signal into an analog signal. The analog signal has a voltage level proportional to the duty cycle of the periodical pulse signal. The periodical pulse signal is generated to control the CPU to be operational between predetermined intervals when the CPU is in an inactive state. A comparator circuit is coupled to the filter circuit for comparing the voltage level of the analog signal with a predetermined voltage level. When the voltage level of the analog signal is below the predetermined voltage level, the comparator circuit generates a switching signal. A switching circuit is coupled to (1) a power supply, (2) the fan, and (3) the comparator circuit for disconnecting the power supply from the fan when the switching signal is generated by the comparator circuit so as to substantially reduce the power consumption of the fan in the computer system when the CPU is in the inactive state. A computer system having the circuit for controlling power consumption of a fan in the system and a method for controlling power consumption of a fan in a computer system are also described.

2/4 PLUSPAT - (C) QUESTEL-ORBIT- image

CPIM (C) Questel-Orbit

PN - US5483464 A 19960109 [US5483464]
KR9505216 B1 19950522 [KR9505216]

TI - (A) Power saving apparatus for use in peripheral equipment of a computer

PA - (A) SAMSUNG ELECTRONICS CO LTD (KR)

IN - (A) SONG MOON-JONG (KR)

AP - 1993US-0176450; 1993KR-0005332

PR - 1993KR-0005332

CT - (US5483464)

US4365290; US4591914; US4593349; US4667289; US4674031; US4677566;
US4747041; US5059961; US5163124; US5175845; US5214785; US5237692;
US5249298; US5251320; US5293494; US5347167; US5375245; US5384721;
US5408668

AB - (US5483464)

An apparatus for use in the peripheral equipment of a computer reduces the needless consumption of power. Once it has been determined that the computer has not been used for a predetermined period of time, an operation control signal indicative of a specific control mode is supplied for controlling the supply of power to the computer's peripheral equipment and the computer's operating state. The operation of a power supply means for generating operating power to a computer's peripheral equipment is controlled in response to a detected control mode. Accordingly, energy is conserved by controlling the supply of power and the operating state of a computer's peripheral equipment according to the peripheral equipment's operational state.

3/4 PLUSPAT - (C) QUESTEL-ORBIT- image

CPIM (C) Questel-Orbit

PN - US5167024 A 19921124 [US5167024]
 AU6016890 A 19910314 [AU9060168]
 AU629019 B2 19920924 [AU-629019]
 CA2024552 A1 19910309 [CA2024552]
 DE4028175 A1 19910321 [DE4028175]
 GB9018259 D0 19901003 [GB9018259]
 GB2235797 A 19910313 [GB2235797]
 GB2235797 B 19930818 [GB2235797]
 HK36394 A 19940429 [HK9400363]
 JP3171317 A 19910724 [JP03171317]
 SE9002838 D0 19900906 [SE9002838]
 SE9002838 A 19910309 [SE9002838]
 SG7294 G 19940610 [SG9400072]

TI - (A) Power management for a laptop computer with slow and sleep modes
 OTI - (A1) ENERGIEMANAGEMENTANORDNUNG FUER EINEN TRAGBAREN COMPUTER
 PA - (A) APPLE COMPUTER (US)
 IN - (A) SMITH R STEVEN (US); HANLON MIKE S (US); BAILEY ROBERT L (US)
 AP - 1992US-0845781; 1990SE-0002838; 1990AU-0060168; 1990DE-4028175;
 1994SG-0000072; 1994HK-0000363; 1990CA-2024552; 1990GB-0018259;
 1990JP-0237294
 PR - 1989US-0405637; 1992US-0845781; 1994SG-0000072
 CT - (US5167024)
 US4019068; US4074351; US4151611; US4279020; US4293927; US4317181;
 US4381552; US4409665; US4611289; US4615005; US4698748; US4712196;
 US4747041; US4809163; US4851987; US4907150; US4980836; EP1723394

AB - (US5167024)
 A power manager within a portable laptop computer provides power and clocking control to various units within the computer in order to conserve battery power. Transistor switches controlled by the power manager control the distribution of power and/or clock signals to the various units within the computer. The power manager includes a software routine for continually monitoring the various units and when these units are either not needed and/or not currently in use, power and/or clock signals are removed from a given unit.

4/4 PLUSPAT - (C) QUESTEL-ORBIT- image
 CPIM (C) Questel-Orbit

PN - US4683382 A 19870728 [US4683382]
 DE3481957 D1 19900517 [DE3481957]
 EP0157905 A2 19851016 [EP-157905]
 EP0157905 A3 19870729 [EP-157905]
 EP0157905 B1 19900411 [EP-157905]
 JP60176121 A 19850910 [JP60176121]
 JP5047848 B 19930719 [JP93047848]
 JP1838072 C 19940411 [JP1838072]

TI - (A) Power-saving voltage supply
 OTI - (A2) Halbleiteranordnung.
 - (A2) Dispositif semi-conducteur.

PA - (A) TOKYO SHIBAURA ELECTRIC CO (JP)
 IN - (A) SAKURAI TAKAYASU (JP); IIZUKA TETSUYA (JP)
 AP - 1984US-0667417; 1984DE-3481957; 1984EP-0113078; 1984JP-0032068
 PR - 1984JP-0032068
 CT - (US4683382)
 US4580063; US4581551
 - Mano et al., "Submission VLSI Memory Circuits," ISSCC Digest of Technical Papers, pp. 234-235, Feb. 1983.
 Itoh et al., "An Experimental IBM DRAW with On-Chip Voltage Limiter," ISSCC Digest of Technical Papers, pp. 282-283, Feb. 1983.

CT - (EP-157905)
 Cited in the search report

- US4054830 (A) (Cat. A);US4390833 (A) (Cat. A);GB2034937 (A) (Cat. A);EP63483 (A) (Cat. A)
- PATENT ABSTRACTS OF JAPAN, vol. 6, no. 34 (P-104) [912], 2nd March 1982; & JP-A-56 153 415 (SHINDENGEN KOGYO K.K.) 27-11-1981 (Cat. X)
- PATENT ABSTRACTS OF JAPAN, vol. 3, no. 156, 21st December 1979, page 43 E 161; & JP-A-54 137 246 (OKI DENKI KOGYO K.K.) 24-10-1979 (Cat. A)
- MOTOROLA TECHNICAL DEVELOPMENTS, vol. 2, January 1982, page 30, Motorola, Schaumburg, Illinois, US; LAL SOOD: "Circuit for reducing standby power for a memory device" (Cat. A)

AB - (US4683382)

In a semiconductor device according to the invention, first and second voltage dropping circuits, for generating voltages respectively having smaller values than that of an external power supply voltage, are provided. The first voltage dropping circuit, which consumes relatively less power, is always in the operative mode, and the second voltage dropping circuit, which consumes more power than that of the first voltage dropping circuit, is operated during an interval other than a standby interval. The voltages generated by the first and second voltage dropping circuits are supplied to an internal power supply line in parallel with each other.